

*3rd Sem (Regular & Back)*

DEC EC- 2011

(CSE, IT, CSCE, CSSE)

**AUTUMN END SEMESTER EXAMINATION-2018**

3rd Semester B.Tech & B.Tech Dual Degree

**Digital electronics**

**ec- 2011**

(Regular- 2017Admitted Batch)

Time: 3 Hours Full Marks: 50

***Answer any FIVE questions including question No.1 which is compulsory.***

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.*

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| 1. |  |  | [110] |
|  | (a) | Perform the BCD addition |  |
|  | (b) | Define “positive logic system” and “negative logic system”. |  |
|  | (c) | Implement the function of 2-input XNOR gate using only 2-input NAND gates. |  |
|  | (d) | Show that |  |
|  | (e) | Implement the function of a NOT gate using 2X1 multiplexer. |  |
|  | (f) | State the difference between asynchronous and synchronous counters. |  |
|  | (g) | Draw the logic diagram of a full-subtractor using two half-subtractors. |  |
|  | (h) | Draw the circuit diagram of a CMOS Inverter. |  |
|  | (i) | Define the term: (i) Fan-in and (ii) Fan-out |  |
|  | (j) | How does a JK flip-flop differ from an SR flip-flop in its operation? What is its advantage over an SR flip-flop? |  |
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| 2. | (a) | Find the minimized expression for the following 4-variable Boolean function using K-map and implement the minimized expression using minimum number of NAND gates only. | [4] |
|  | (b) | Design a 4-bit ADDER-SUBTRACTOR circuit using Full-adders and 2-input XOR gates only. Explain briefly its operation. | [4] |
|  | (c) | State the differences between Mealy model and Moore model. | [2] |
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| 3. | (a) | What is a priority encoder? Design a 4:2 priority encoder such that the order of priority of the decimal inputs is given as , where all are inputs to the encoder. | [5] |
|  | (b) | Explain the working of R-2R Ladder type DAC with an appropriate diagram. | [5] |
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| 4. | (a) | Design a full-adder using 3-line-to-8 line decoder (active HIGH output lines) and logic gates only. | [4] |
|  | (b) | Design a JK flip-flop using a D flip-flop and 2-input logic gates. | [4] |
|  | (c) | Design an asynchronous 2-bit Up counter using negative-edge triggered JK flip-flops. Also draw the timing diagram of this counter. | [2] |
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| 5. | (a) | Design a synchronous counter using T flip-flops that goes through the following binary repeated sequence: 0,1,2,3,4,5,6,7,0,1,2,3,4,5,6,7,… | [5] |
|  | (b) | Design a MOD-8 Johnson counter and a MOD-4 Ring counter. Write the sequence of states for each of these counters. | [5] |
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| 6. | (a) | Design a 4-bit SISO Shift Register using D flip-flops. Assume that a 4-bit data 0101 is entered serially into the register, write the sequence of states in case of right shift operation. | [4] |
|  | (b) | Implement the following Boolean function with 8X1 Multiplexer. | [4] |
|  | (c) | Design a 2-line-to-4 line decoder (active LOW output lines and active LOW Enable input) circuit using NAND gates only. | [2] |
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| 7. | (a) | Design a Mealy type synchronous sequential circuit using D flip-flops which produces output Z = 1 when binary sequence “1010” is detected. Assume overlapping is permitted. | [5] |
|  | (b) | With the help of a neat diagram, explain the working of a two input TTL NAND gate. State the advantages and disadvantages of Totem Pole output configuration in the circuit of TTL NAND gate. | [5] |
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| 8. | (a) | An 8X1 multiplexer has inputs A, B and C connected to the selection inputs and respectively. The data inputs through are as follows:  and  Determine the Boolean function that the multiplexer implements. | [4] |
|  | (b) | Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is an even number. | [4] |
|  | (c) | Draw the Mealy model and Moore model of the state diagrams of SR flip-flop. | [2] |
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